HiperLAN 5.4 GHz Low Power CMOS Synchronous Oscillator

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***Abstract* — A 5.4 GHz 0.25 µm VLSI CMOS Synchronous Oscillator is proposed, which is designed to act as a local oscillator for HiperLAN systems. The design strategy is described, including the synchronization range optimization approach. A chip is presented, which provides a 150 MHz synchronization range and a -97dBc/Hz phase noise at 10 kHz offset from the carrier, while only consuming 5 mA from a 2.5 V supply.**

I. Introduction

The new HiperLAN standard defines a frequency band from 5.15 GHz up to 5.25 GHz for the future RF digital data transmission systems. While a 100 MHz wide frequency band centered at roughly 5 GHz is not a stringent constraint, so high a frequency of interest will doubtless induce large power consumption within the frequency synthesizer. This will mostly be due to the frequency dividers. In addition, for the dividers to be able to handle 5 GHz signals, advanced technologies are mandated. Thus, making both low-cost and low-power systems will be difficult to achieve, if not impossible.

On the other hand, Synchronous Oscillators (SO) based synthesizers had been previously proposed as an alternative to Phase Locked Loop (PLL) based synthesizer [1-2]. Indeed, the injection-locked phenomena SO takes advantage of leads to very compact PLL-like circuits. As no further frequency divider is needed in a SO, power consumption is dramatically reduced with regards to its PLL counterparts, and classical technologies such as VLSI CMOS can still be brought into play.

This paper presents a 5.4 GHz Synchronous Oscillator which is implemented in such a VLSI CMOS technology. The circuit is designed to act as a local oscillator in a superheterodyne HiperLAN receiver with a 200 MHz intermediate frequency. Based on a SO theory derived from [3], the design strategy leading to an optimized SO is first proposed. Second, the chip is described and third, experimental results are given which highlight the excellent behavior of the circuit.

II. Design Strategy

A. Theoretical synchronization range

The theory proposed in [3] can be adapted to suit for modern microelectronic circuits with only minor changes. It leads to the synchronization range of the SO, a property similar to the lock range of PLL [4] :

$$\Delta f = 2 \cdot \frac{\left| I_{sync} \right|}{\left| V_{osc} \right|} \cdot \sqrt{F_g^2 + F_b^2} \qquad (1)$$

where Δf is the synchronization range, I_{sync} the synchronization current, V_{osc} the free running oscillation amplitude, and F_g and F_b the so-called 'compliance factors' which are respectively the sensitivities of the oscillator frequency with regards to variations in the real and imaginary parts of the LC-tank impedance.

B. Bandwidth optimization

Thanks to the theory, an expression of the SO bandwidth BW is obtained :

$$BW = \frac{\Delta f}{2} \cdot \sin\left(\arccos\left(\frac{2\left(f_1 - f_0 \right)}{\Delta f} \right) \right) \qquad (2)$$

where Δf is the synchronization range, f_0 the free running oscillation frequency and f_1 the synchronization signal frequency. Within this bandwidth, the SO merely copies the synchronization signal phase noise. Due to stability reasons, BW is always positive.

Unlike PLL, (2) exposes that a SO bandwidth is strongly related to its locked frequency. However, with Δf classical values, BW is always in the range of a few tens of megahertz. Such a characteristic is very difficult to obtain in PLL systems [4], even with fractional dividers [5].

As a matter of consequence, the larger the synchronization range the lower the SO based synthesizer phase noise can be. Eq. 1 demonstrates that it can be obtained with both large compliance factors and large synchronization current.

C. Compliance factors optimization

A compliance factors computation for usual oscillator architectures establishes that, among these architectures, both Colpitts and 'negative-resistor' topologies are providing the largest synchronization range. Nonetheless, the latter was preferred as the negative-resistor oscillator differential nature adds substrate coupling immunity for free.

The oscillator schematic is depicted in Fig. 1.

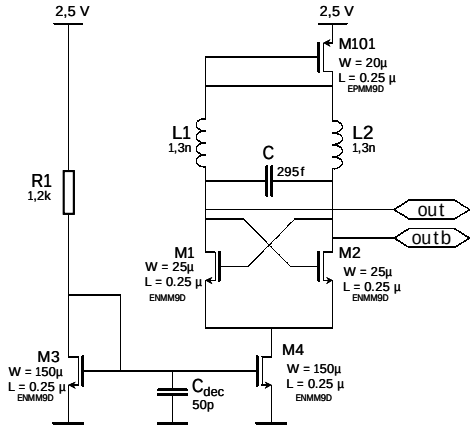

Fig. 1. The negative resistor oscillator.

The first order synchronization range for the circuit in Fig. 1 is then given by (3) :

$$\Delta f = \frac{1}{2\pi} \cdot \frac{\left| I_{sync} \right|}{\left| V_{osc} \right|} \cdot \frac{1}{C} \qquad (3)$$

with C the overall tank capacitor, including parasitic. A trade-off between inductance parameters, power consumption and self resonance effects leads to the components values shown in Fig. 1. Its yields a 600 mV differential free running oscillation amplitude, and a roughly 5.4 GHz free running frequency.

D. Synchronization current optimization

We are looking for a sub-harmonic synchronization process [1], with a 450 MHz synchronization signal to lock the SO at 5.4 GHz, the 12th harmonic. Hence, the synchronization current waveform has been chosen as depicted in Fig. 2.

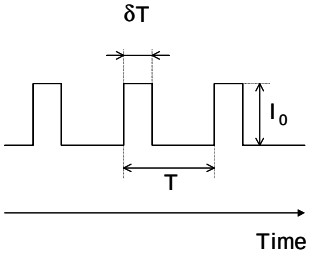

Fig. 2. The synchronization current waveform.

Such a waveform has a n[th] harmonic amplitude of :

$$I_n = \frac{I_0 \sqrt{2}}{n\pi} \cdot \sqrt{1 - \cos\left(2n\delta\pi\right)} \qquad (4)$$

A maximum is obtained when the pulse duration is exactly 50% of the SO output signal period. With the components values of Fig. 1, a 400 µA 12th harmonic current amplitude is needed to provide a 150 MHz frequency range, which is well suited for our HiperLAN application - including a margin. It imposes a 4 mA current pulse at the wanted 450 MHz synchronization signal frequency.

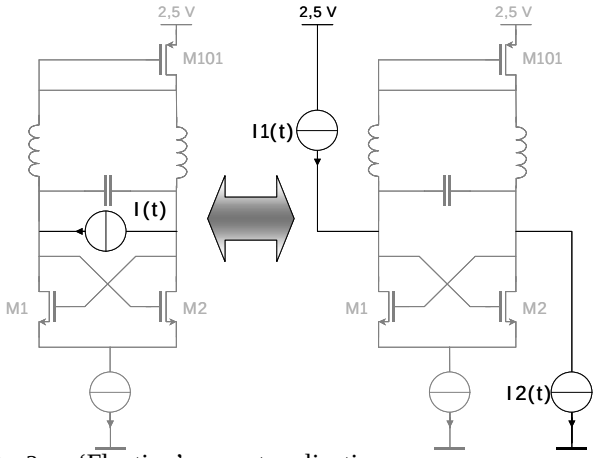

Fig. 3. 'Floating' current realization

Fig. 3 emphasizes the way we design the 'floating' current synchronization source *I(t)* with two asymmetric current sources $I_1(t)$ and $I_2(t)$. While this approach reduces the differential advantage, it is far easier to implement. It is the reason why M_{101} was added in the negative resistor oscillator, as it provides voltage headroom for the $I_1(t)$ PMOS current switch.

Fig. 4 depicted the current pulse generator, based on a Delay Oriented Design (DOD) approach.

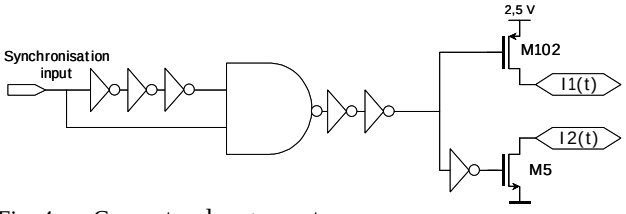

Fig. 4. Current pulse generator

E. The overall synchronous oscillator

Both the NAND and inverters MOSFET dimensions in Fig. 4 were carefully chosen so as to provide a 4 mA output current pulse duration of around 100 ps, in good agreement with the optimum value given by (4). It yields a 12th harmonic current amplitude of 420 µA, leading to a theoretical synchronization range of 160 MHz, according

to the abovementioned 600 mV differential free running oscillation amplitude.

In these conditions, the overall SO – *ie* the negative resistor oscillator of Fig. 1 and the current pulse generator of Fig. 4 – sinks 3 mA from the 2.5 V voltage supply. According to (2), the bandwidth of this SO in the HiperLAN frequency range is always larger than 50 MHz. Hence, though the SO is a PLL-like system, its characteristics largely outclass those of a real PLL.

III. The 0.25 µm CMOS Chip

A chip was manufactured in STMicroelectronics HCMOS7 technology, a 0.25 µm CMOS technology with 6 interconnection layers.

The hollow spiral inductors were designed with the last two metal layers in parallel, leading to a quality factor of roughly 5 due to the low resistivity CMOS substrate.

The LC-tank capacitor quality factor is as important as the inductor one. To avoid both the low quality factor associated to polysilicon capacitors as well as non-VLSI and thus expensive technology steps, the tuning capacitor was designed as a pseudo-fractal lateral flux capacitor [1], [6]. Practically, two series capacitors were used to help maintaining the differential nature of the negative resistor oscillator.

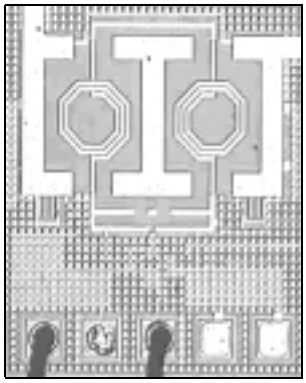

Fig. 5. The chip microphotograph

Fig. 5 depicts the chip microphotograph. One can see both the two hollow spiral inductors and the two lateral flux capacitors. Most of the remaining circuit parts are covered by dummy metals, which are mandated to preserve chip planarisation.

IV. Experimental Results

The chip was encapsulated in a TQFP32 classical plastic package, and soldered on a specific PCB in low cost FR2 epoxy. Measurements were then performed with a HP8563E spectrum analyzer, and with a HP8648 signal generator whenever synchronization was needed. Indeed, the generator provides a sinusoidal signal of around 450 MHz which acts as the synchronization signal for the SO to synchronize on the 12^{th} harmonic, at roughly 5.4 GHz. The DC voltage bias is 2.5 V.

A. Free running oscillator

In free running mode, a DC current consumption of 42 mA was measured. The two 50 Ω buffers included within the chip are the major culprit, as they are expected from simulation to sink more or less 20 mA each. It yields a current consumption of 2 to 3 mA for the oscillator, in good agreement with simulations.

The free running frequency is measured at 5.405 GHz, and the spectrum is depicted in Fig. 6.

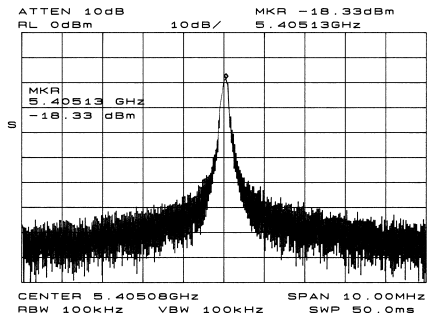

Fig. 6. Free running spectrum

The SSB phase noise is depicted in Fig. 7.

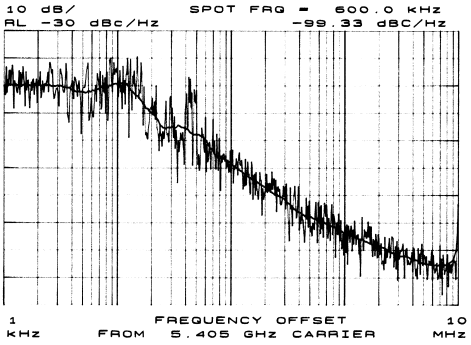

Fig. 7. Free running SSB phase noise

While this phase noise should have little influence according to the 50 MHz of expected bandwidth, one can observe a –99 dBc/Hz spot at a 600 kHz offset from the carrier. This is not so bad a value with regards to the low power consumption behavior.

B. Synchronized oscillator

While synchronization is brought into play, a 2 mA increase in DC current consumption is observed. It is due to the synchronization network, which is no longer idle.

A 450 MHz input signal leads to the 5.4 GHz SO output signal which spectrum is illustrated in Fig. 8.

The 1 kHz per division at 5.4 GHz horizontal scale of Fig. 8 highlights the excellent stability of the SO in terms of frequency. The SSB phase noise depicted in Fig. 9 is a mere corroboration of this attribute. Indeed, a –97 dBc/Hz spot at 10 kHz offset of the carrier is obtained, *ie* a significant value for a full VLSI and low-power CMOS circuit.

The measured synchronization range coarsely spread from 444 MHz up to 456 MHZ for the input synchronization signal, corresponding to a 5.325 GHz up to 5.475 GHz SO output signal. Thus a 150 MHz range is observed, while a 160 MHz was expected, leading to a 7% error. Taking into account the passive components dispersion, it is in good agreement with simulation results, and it stays HiperLAN compatible.

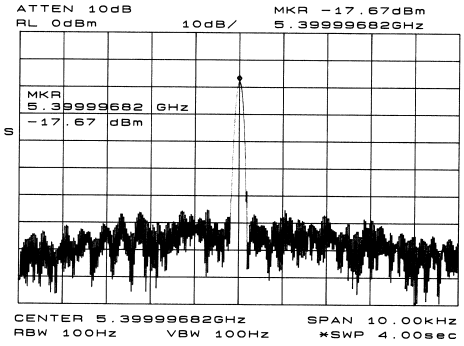

Fig. 8. Synchronized spectrum

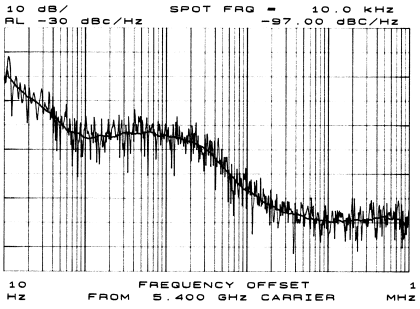

Fig. 9. Synchronized SSB phase noise

C. Phase noise consideration - Limitations

As a matter of fact, the phase noise of the synchronization signal is mostly significant in the SO phase noise performance. Indeed, as a classical PLL does, the SO phase noise is a bare copy of the synchronization signal one, shifted by the log conversion of the frequency division ratio.

Hence, whenever a noisy synchronization signal is used, a high SO phase noise can be observed. Nevertheless, since it is obviously easier to obtain a low phase noise signal at low frequency than in the RF frequency range, as some compensation techniques can be implemented, the combination of both a low-frequency low-phase noise reference and this SO yields to a low-power, low-phase noise and low-cost frequency synthesizer.

V. Conclusion

A 5.4 GHz full VLSI 0.25 µm CMOS Synchronous Oscillator has been presented. This SO is well suited to fulfill a low-power frequency synthesizer able to deal with HiperLAN requirements. The major measured characteristics of the chip are summarized in Table I.

TABLE I
SUMMARY OF SO CHARACTERISTICS

Technology	0.25 µm VLSI CMOS
Supply voltage	2.5 V
Output center frequency	5.4 GHz
Free running phase noise	-99 dBc/Hz @ 600 kHz
Input frequency	444 MHz to 456 MHz
Synchronization range	5.325 GHz to 5.475 GHz
SO current - synchronized	5 mA
Synchronized phase noise	-97 dBc/Hz @ 10 kHz (depending on reference)

Thanks to the very wide bandwidth of the SO, the oscillator performances are no longer of any interest, at least as long as it is still able of oscillations. So, a dramatic reduction in current consumption can be achieve, as the oscillator phase noise optimization is not mandated anymore. In addition, VLSI CMOS technologies appear efficient, paving the way to low-cost RF systems which are required to sustain as well as to strengthen the present wireless revolution.

References

[1] F. Badets, Y. Deval, J-B. Bégueret, A. Spataro and P. Fouillat, "A 2.7 V 2.64 GHz Fully Integrated Synchronous Oscillator for WLAN Applications", *Proc. of the 25th European Solid-State Circuits Conf. (ESSCIRC'99)*, Duisburg, Germany, September 1999, pp. 210-213.

[2] F. Badets, Y. Deval, J-B. Bégueret, A. Spataro and P. Fouillat, "A 3 V 2.3 GHz Fully Integrated Synchronous Oscillator for WLAN Applications", *IEEE Proc. of the Bipolar/BiCMOS Circuits and Tech. Meeting (BCTM'99)*, Minneapolis, MN, USA, September 1999, pp. 145-148.

[3] R. Huntoon and A. Weiss, "Synchronisation of Oscillators", *Proc. of the I.R.E.*, December 1947, vol. 35, pp. 1415-1423.

[4] U. L. Rhode, *Microwave and Wireless Synthesizer*, John Wiley & Sons, New York, NY, USA, 1997.

[5] J. A. Crawford, *Frequency Synthesizer Design Handbook*, Artech House Inc., Norwood, MA, USA, 1994.

[6] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, Cambridge, UK, 1998.